What is claimed is:

1. A response time accelerator for driving a liquid crystal display (LCD) comprising:

a frame memory unit that updates and stores one or more frames of previous data;

a table memory unit that stores predetermined mapped panel output values, predetermined mapped panel characteristic values, and flag information corresponding to the predetermined mapped panel characteristic values; and

an acceleration unit that reads the previous data corresponding to input current data and reads and decodes the predetermined mapped panel output value, predetermined mapped panel characteristic value, and flag information corresponding to the previous data and current data, performs interpolations on the decoded mapped panel output value and mapped panel characteristic value according to the flag information, and generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit.

2. The response time accelerator of claim 1, wherein the acceleration unit comprises:

a comparator that compares the current data with the previous data and outputs the liquid crystal panel data and the previous data of the next frame with the same value as the current data, or the current data and the previous data;

a coefficient generator that generates coefficients to be used for interpolation based on the current data and previous data;

a table decoder that reads and decodes the predetermined mapped panel output value, predetermined mapped panel characteristic value, and flag information corresponding to the previous data and current data;

a panel output interpolator that performs interpolation on the decoded predetermined mapped panel output value and generates the liquid crystal panel data;

a frame memory output interpolator that performs interpolation on the decoded predetermined panel characteristic value and generates the previous data of the next frame;

a panel output selector that selectively receives the output of the comparator or the output of the panel output interpolator and outputs the liquid crystal panel data; and

a frame memory output selector that selectively receives the output of the comparator or output of the frame memory output interpolator and outputs the previous data of the next frame.

3. The response time accelerator of claim 1, wherein the flag information is in a first logic state when the current data is the same as the previous data of the next frame, and in a second logic state when the current data is different from the previous data of the next frame.

4. The response time accelerator of claim 2, wherein the flag information is in a first logic state when the current data is the same as the previous data of the next frame, and in a second logic state when the current data is different from the previous data of the next frame.

5. The response time accelerator of claim 1, wherein the interpolation is performed using the following equation:

l=Pn-1[DB-1:DB-n]

m=Pn[DB-1:DB-n]

r=Pn-1[DB-(n+1):0]

s=Pn[DB-(n+1):0]

$A=\{TP(l,m)*(2^{(DB-n)}-r)+TP(l+1,m)*r\}\gg(DB-n)$

$C=\{TP(l,m+1)\ (2^{(DB-n)}-r)+TP(l+1,m+1)*r\}\gg(DB-n)$

$PZ=\{A*\ (2^{(DB-n)}-s)+C*s\}\gg(DB-n)$

where Pn, Pn-1, and TP denote the current data, previous data, and a mapped panel output value or a mapped panel characteristic value, respectively, and DB, n, and PZ are the number of data bits, the number of bits after truncation, and an output value, respectively.

6. The response time accelerator of claim 2, wherein the interpolation is performed using the following equation:

$l=Pn\text{-}1[DB\text{-}1:DB\text{-}n]$

$m=Pn[DB\text{-}1:DB\text{-}n]$

$r=Pn\text{-}1[DB\text{-}(n+1):0]$

$s=Pn[DB\text{-}(n+1):0]$

$A=\{TP(l,m)*(2^{(DB-n)}-r)+TP(l+1,m)*r\}\gg(DB-n)$

$C=\{TP(l,m+1)\ (2^{(DB-n)}-r)+TP(l+1,m+1)*r\}\gg(DB-n)$

$PZ=\{A*\ (2^{(DB-n)}-s)+C*s\}\gg(DB-n)$

where Pn, Pn-1, and TP denote the current data, previous data, and a mapped panel output value or a mapped panel characteristic value, respectively, and DB, n, and PZ are the number of data bits, the number of bits after truncation, and an output value, respectively.

7. The response time accelerator of claim 1, wherein in performing the interpolation when the flag information is in a second logic state, the liquid crystal panel data is obtained by interpolation at a minimum gray level value if the most significant bit

(MSB) of the current data is in a first logic state and at a maximum gray level value if the MSB of the current data is in a second logic state.

8. The response time accelerator of claim 2, wherein in performing the interpolation when the flag information is in a second logic state, the liquid crystal panel data is obtained by interpolation at a minimum gray level value if the most significant bit (MSB) of the current data is in a first logic state and at a maximum gray level value if the MSB of the current data is in a second logic state.

9. The response time accelerator of claim 1, wherein the predetermined mapped panel output values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

10. The response time accelerator of claim 2, wherein the predetermined mapped panel output values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

11. The response time accelerator of claim 1, wherein the predetermined mapped panel characteristic values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

12. The response time accelerator of claim 2, wherein the predetermined mapped panel characteristic values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

13. The response time accelerator of claim 2, wherein the comparison is performed using the following equation:

$$|(Pn-1)-(Pn)| \leq THV \rightarrow PO = Pn, pPn = Pn$$

where Pn-1, Pn, and THV denote the previous data, the current data, and a predetermined threshold value, respectively, and PO and pPn are the liquid crystal panel data and previous data of the next frame.

14. A method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data, a table memory unit for storing predetermined mapped panel output values, predetermined mapped panel characteristic values, and flag information corresponding to the predetermined mapped panel characteristic values, and an acceleration unit for generating data to be output to the liquid crystal panel, the method comprising the steps of:

receiving current data in the acceleration unit;

reading the previous data corresponding to the current data in the acceleration unit;

reading and decoding the predetermined mapped panel output value, predetermined mapped panel characteristic value, and flag information corresponding to the previous data and current data in the acceleration unit;

performing interpolation on the decoded predetermined mapped panel output value according to the flag information and generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit; and

performing interpolation on the decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit.

15. The method of claim 14, further comprising the step of comparing the current data with the previous data and outputting the liquid crystal panel data and previous data of the next frame with the same value as the current data, or the current data and previous data.

16. The method of claim 14, wherein the flag information is in a first logic state when the current data is the same as the previous data of the next frame, and in a second logic state when the current data is different from the previous data of the next frame.

17. The method of claim 14, wherein the interpolation is performed using the following equation:

$I=Pn\text{-}1[DB\text{-}1:DB\text{-}n]$

$m=Pn[DB\text{-}1:DB\text{-}n]$

$r=Pn\text{-}1[DB\text{-}(n+1):0]$

$s=Pn[DB\text{-}(n+1):0]$

$A=\{TP(I,m)*(2^{(DB-n)}-r)+TP(I+1,m)*r\}\gg(DB-n)$

$C=\{TP(I,m+1)\ (2^{(DB-n)}-r)+TP(I+1,m+1)*r\}\gg(DB-n)$

$PZ=\{A*\ (2^{(DB-n)}-s)+C*s\}\gg(DB-n)$

where Pn, Pn-1, and TP denote the current data, previous data, and a mapped panel output value or a mapped panel characteristic value, respectively, and DB, n, and PZ are the number of data bits, the number of bits after truncation, and an output value, respectively.

18. The method of claim 14, wherein in performing the interpolation when the flag information is in a second logic state, the liquid crystal panel data is obtained by

interpolation at a minimum gray level value if the most significant bit (MSB) of the current data is in a first logic state and at a maximum gray level value if the MSB of the current data is in a second logic state.

19. The method of claim 14, wherein the predetermined mapped panel output values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

20. The method of claim 14, wherein the predetermined mapped panel characteristic values correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

21. The method of claim 11, wherein the comparison is performed using the following equation:

$$\left|(Pn-1)-(Pn)\right| \le THV \rightarrow PO = Pn, pPn = Pn$$

where Pn-1, Pn, and THV denote the previous data, the current data, and a predetermined threshold value, respectively, and PO and pPn are the liquid crystal panel data and previous data of the next frame.